



Attorney Docket No.: CYPR-CD00232

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**  
**Patent Application**

Inventor(s): Warren Snyder

Serial No.: 10/033,027

Filed: 10/01/01

Title: PROGRAMMABLE SYSTEM ON A CHIP

Group Art Unit:

Examiner:

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**MAR 03 2003**

**Technology Center 2100**

**Form 1449**

**U.S. Patent Documents**

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
W	A	6,144,327	11/07/00	Distinti et al.	341	126	08/12/97
W	B	5,202,687	04/13/93	Distinti	341	158	06/12/91
W	C	6,166,367	12/26/00	Cho	250	208.1	03/26/99
W	D	5,600,262	02/04/97	Kolze	326	38	10/11/95
W	E	5,414,308	05/09/95	Lee et al.	327	293	07/29/92
W	F	5,258,760	11/02/93	Moody et al.	341	166	07/13/92
W	G	5,563,526	10/08/96	Hastings et al.	326	37	01/03/94
W	H	6,225,866	05/01/01	Kubota et al.	330	295	06/14/00
W	I	5,880,598	03/09/99	Duong	326	41	01/10/97
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W	M	5,703,871	12/30/97	Pope et al.	370	248	05/26/95
W	N	6,018,559	01/25/00	Azegami et al.	377	79	12/16/96
W	O	6,191,660	02/20/01	Mar et al.	331	111	03/24/99
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**Foreign Patent or Published Foreign Patent Application**

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation	
							Yes	No
	T							



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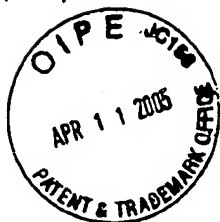
MAR 03 2003

Technology Center 2100

## Related Pending US Patent Applications

Examiner Initial	No.	Docket Number, Title, Filing Date, Serial Number & Inventors
	U	CYPR-CD00169; "PROGRAMMABLE MICROCONTROLLER ARCHITECTURE (MIXED ANALOG/DIGITAL)"; 08/07/01; 09/924,734; Snyder et al.
	V	CYPR-CD00170; "DIGITAL CONFIGURABLE MACRO ARCHITECTURE"; 07/18/01; 09/909,045; W. Snyder
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	X	CYPR-CD00173; "A PROGRAMMABLE ANALOG SYSTEM ARCHITECTURE (AS AMENDED)"; 07/18/01; 09/909,047; M. Mar
	Y	CYPR-CD00174; "PROGRAMMING METHODOLOGY AND ARCHITECTURE FOR A PROGRAMMABLE ANALOG SYSTEM (AS AMENDED)"; 08/14/01; 09/930,021; Mar et al.
	Z	CYPR-CD00175; "METHOD FOR SYNCHRONIZING AND RESETTING CLOCK SIGNALS SUPPLIED TO MULTIPLE PROGRAMMABLE ANALOG BLOCKS (AS AMENDED)"; 10/01/01; 09/969,311; B. Sullam
	AA	CYPR-CD00180; "METHOD AND APPARATUS FOR PROGRAMMING A FLASH MEMORY"; 06/05/01; 09/875,599; W. Snyder
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	CC	CYPR-CD00187; "A CONFIGURABLE INPUT/OUTPUT INTERFACE FOR A MICROCONTROLLER"; 09/14/01; 09/953,423; Kutz et al.
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Examiner	Date Considered	

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.



Attorney Docket No.: CYPR-CD00232

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**  
**Patent Application**

Inventor(s): Snyder

Group Art Unit: 2183

Filed: October 22, 2001

Examiner: PAN, Daniel H.

Application No.: 10/033,027

Confirmation No.: 8635

Title: PROGRAMMABLE SYSTEM ON A CHIP

**Form 1449**

**U.S. Patent Documents**

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	A	5,399,922	3/21/95	Kiani et al.	326	40	7/2/93
	B	5,680,070	10/21/97	Anderson et al.	327	336	2/5/96
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Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation	
							Yes	No
	L	0450863A2	10/9/91	EPO	G11C	27/02		
	M	0499383A2	8/19/92	EPO	H03K	19/177		
	N	0308583 A2	3/29/89	EPO	G06J	1/00		
	O	069816A2	2/22/95	EPO	G06J	1/00		
	P	1170671A1	1/8/02	EPO	G06F	17/13		
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**Other Documents**

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	R	Goodenough, F. "Analog Counterparts of FPGAS Ease System Design" Electronic Design, Penton Publishing Cleveland, OH, US vol. 42, no. 21, 10/14/94, pages 63-64, 66,68,7 XP000477345 ISSN: 0013-4872 the whole document.
	S	Harbaum T. El. Al: "Design of a Flexible Coprocessor Unit" Proceedings of the Euromicro Conference, XX XX, Sept. 1999, pages 335-342, XP000879556, page 337, right-hand column, line 13-page 338, left hand column, line 4; figure 1.
Examiner		Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered.  
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Patent Application

Inventor(s): Warren Snyder

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Title: PROGRAMMABLE MICROCONTROLLER ARCHITECTURE

**Form 1449**

**U.S. Patent Documents**

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
<u>W</u>	A	6,460,172	10/01/02	Insenser Farre et al.	716	17	06/21/00

**Foreign Patent or Published Foreign Patent Application**

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation	
							Yes	No
	B							

**Other Documents**

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	C	
Examiner	Date Considered	

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